

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: **Bera, et al.**

Case: **8477/ETCH/DRIE**

Serial No.: **10/663,304**

Filed: **September 16, 2003**

Examiner: **Pham, Thanh V.**

Group Art Unit: **2823**

Confirmation No.: **1356**

Title: **METHOD OF FABRICATING A DUAL DAMASCENE
INTERCONNECT STRUCTURE**

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

Pursuant to the Examiner's Answer dated on March 20, 2007, the Appellants submit this Reply Brief to the Board of Patent Appeals and Interferences. The Appellants believe that no fees are due in connection with this submission. However, the Commissioner is hereby authorized to charge counsel's Deposit Account No. 50-3562 for any fees, including extension of time fees, required to make this response timely and acceptable to the Office.

REAL PARTY IN INTEREST

The real party in interest is Applied Materials, Inc., located in Santa Clara, California.

RELATED APPEALS AND INTERFERENCES

The Appellants know of no related appeal and/or interference that may directly affect or be directly effected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-17 and 40-45 are pending in the application. Claims 1-17 and 40-45 stand rejected in view of several references as discussed below. The rejection of claims 1-17 and 40-45 based on the cited references is appealed. The pending claims are shown in the attached Appendix.

STATUS OF AMENDMENTS

No amendments to the claims were submitted in this application subsequent to final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention provides a method for fabricating a dual damascene interconnect structure. In the embodiment of independent claim 1, a method of fabricating an interconnect structure comprises (a) providing a substrate 200 having a film stack 201 comprising sequentially formed on the substrate 200 a first barrier layer 202, a conductive layer 216 embedded in a first dielectric layer 204, a second barrier layer 206, a second dielectric layer 208, and a cap layer 210 (*Specification*, ¶ [0018]; Figs. 1, 2A); (b) etching a via hole 224 in the cap layer 210 and the second dielectric layer 208 (*Id.*, ¶ [0025]; Figs. 1, 2C); (c) filling a portion of a depth 226 of the via hole 224 with a masking material (*Id.*, ¶ [0028]; Figs. 1, 2E); (d) etching in-situ the cap layer 210 (*Id.*, ¶ [0033]-[0034]; Figs. 1, 2H), a trench 218 in the second dielectric layer 208 (*Id.*, ¶ [0035]-[0036]; Figs. 1, 2I), the masking material (*Id.*, ¶ [0037]-[0038]; Figs. 1, 2J),

and the second barrier layer 206 (*Id.*, ¶ [0039]-[0040]; Figs. 1, 2K), by providing a plasma source power 318 of at least about 1000 Watts and a bias power 322 of at least about 800 Watts while etching during at least a portion of step (d) (*Id.*, ¶ [0036]); and (e) metallizing the via hole 224 and the trench 218 (*Id.*, ¶ [0041]; Figs. 1, 2L).

In the embodiment of independent claim 40, a method of etching comprises (a) providing a substrate 200 having a dielectric layer 204 to be etched on a substrate support 316 in a process chamber 310, the process chamber 310 having a plasma source electrode 328 disposed above the substrate support 316 and a substrate bias electrode disposed below a support surface of the substrate support 316 (*Id.*, ¶ [0018]; Figs. 1, 2A, 3); (b) providing an etch gas mixture 350 (*Id.*, ¶ [0036]; Figs. 1, 2I, 3); and (c) supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode 328 and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer 204 (*Id.*, ¶ [0036]; Figs. 1, 2I, 3).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-6, 8-10 and 40-45 stand rejected under 35 U.S.C. §103(a) as being obvious in light of United States Patent No. 6,797,633, issued September 28, 2004, to *Jiang, et al.* (hereinafter *Jiang*) in view of United States Patent No. 6,797,633, issued July 30, 2002 to *Ikeda* (hereinafter *Ikeda*).

2. Claims 7, 11-17 and 44-45 stand rejected under 35 U.S.C. §103(a) as being obvious in light of *Jiang* in view of *Ma* and/or *Ikeda*, as applied to claims 1-6, 8-10, and 40-45 above, and further in view of Taiwan Patent 544,815 published August 1, 2003 to *Chun, et al.* (hereinafter *Chun*), and United States Patent 6,177,147 issued on January 23, 2001 to *Samukawa, et al.* (hereinafter *Samukawa*).

RESPONSE TO EXAMINER'S ANSWER

1. Claims 1-6, 8-10 and 40-45

The Appellants thank the Examiner for pointing out that the rejection in view of United States Patent Application Publication Serial No. 2004/0161930, published August 19, 2004 to *Ma, et al.* was withdrawn in the Advisory Action dated August 31,

2006. However, the Appellants arguments with respect to the rejection of claims 1-6, 8-10 and 40-45 as being obvious in light of *Jiang* in view of *Ikeda* still stand.

The Appellants addressed the reasons for combining the teachings of *Jiang* and *Ikeda* previously provided in the Final Office Action (regarding reducing fluorine radicals) in the Appeal Brief because it was unclear to the Appellants whether this ground was still be asserted in the subsequent Advisory Action. However, in the Examiner's Answer, the Examiner appears to maintain the rejection of the above-referenced claims under 35 USC §103(a) only by asserting that it would have been obvious to combine the teachings of *Jiang* and *Ikeda* in a manner that yields the claimed limitations because the teachings of *Ikeda* are "useful in etching stacked layers in the formation of the damascene structure." (Examiner's Answer, p. 9, ll. 3-8.)

However, as mentioned in the Appeal Brief filed November 4, 2006 (and in the Corrected Appeal Brief filed January 22, 2007), the MPEP and caselaw provide that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP § 2143.01 (III) (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))(emphasis in original).

As further previously discussed, the MPEP and caselaw provide that Examiners can satisfy this burden "only by showing some objective teaching in the prior art that would lead an individual to combine the relevant teachings of the references." (*In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992); see also, *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143 (Fed. Cir. 1985) (There must be some reason for the combination other than the hindsight gleaned from the invention itself to selectively combine prior art references to render a subsequent invention obvious.))

Here, the Examiner asserts that it would have been obvious to combine *Jiang* and *Ikeda* because *Ikeda* discloses the conditions are "useful" in etching stacked layers. (Examiner's Answer, p. 9, ll. 3-8.) However, the Appellants submit that the teachings of *Ikeda* and *Jiang* would still fail to "lead an individual to combine the relevant teachings of the references," as required by *In re Fritch* (cited above). Specifically, as noted above, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the

combination." *MPEP* § 2143.01 (III) (citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990))(emphasis added).

In this case, the prior art fails to teach or suggest the desirability of the combination. Specifically, neither *Jiang* nor *Ikeda* provide any hint as to the desirability of the combination proposed by the Examiner. For example, the Examiner cites to no portion of *Ikeda*, nor provides any line of reasoning why someone of ordinary skill in the art would replace the conditions specifically taught to be performed in *Jiang* with certain specific process conditions mentioned in *Ikeda*, but not taught or suggested by *Ikeda* to provide any specific benefit or advantage over the conditions taught in *Jiang*.

In other words, and as asserted in the previously submitted Office Action Responses, Appeal Brief, and Corrected Appeal Brief, there is no "suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings," as required to establish a *prima facie* case of obviousness. *MPEP* §2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)).

Accordingly, the Appellants maintain that the Examiner appears to be inadvertently and inappropriately using hindsight analysis to pick and choose teachings from the references to support the obviousness rejection. In the Examiner's Answer, the Examiner agrees that hindsight reasoning must not take into account "knowledge gleaned only from the applicant's disclosure." (*Examiner's Answer*, p. 9, l. 19 – p. 10, l. 5 (citing *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971)).) Similarly, as discussed in the previously filed Appeal Briefs, it is well-settled that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (*In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988)) Thus, the Appellants maintain that the teachings of *Ikeda* cannot be combined with the remaining references in the manner suggested by the Examiner because there is no motivation or suggestion of the desirability of the proposed combination other than what is described in the Appellants present pending Patent Application.

With respect to the Examiner's comment regarding the timeliness of the argument that the Examiner's rebuttal to the arguments against combining *Jiang* and

Ikeda inappropriately presumes the combination (referring to the Office Actions dated November 22, 2005 and February 24, 2006), the Appellants note that this argument was similarly raised in the responses to both office actions, and is thus timely. (See, Response dated December 8, 2005, p. 10, first full ¶; Response dated May 23, 2006, p. 10, second full ¶.)

With respect to the Examiner's comment regarding the recognition of additional advantages of *Ikeda*, the Appellants submit that such arguments were directed towards the Examiner's previously proffered motivation to combine references. Specifically, such arguments were directed towards the proffered motivation to combine the teachings of *Ikeda* in order to reduce fluorine radicals.

In summary, it is respectfully submitted that *Ikeda* fails to teach or suggest a modification to the teachings of *Jiang* that would result in the limitations recited in the present claims. Therefore, a *prima facie* case of obviousness has not been established because any permissible combination of the cited references fails to yield all of the limitations recited in each of independent claims 1 and 40, and all claims respectively depending therefrom.

Thus, independent claims 1 and 40, and claims 2-6, 8-10 and 41-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ikeda*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

2. Claims 7, 11-17 and 44-45

With respect to the Examiner's comments regarding the Appellants' arguments in section 2, relating to the rejection of claims 7, 11-17, and 44-45, the Appellants included such arguments for completeness to show that the consideration of the additional references would still fail to teach or suggest the limitations recited in the claims.

The Appellants thank the Examiner for his comments that neither *Chun* nor *Samukuwa* teaches or suggests the source and bias power limitations missing from the combination of *Jiang* and *Ikeda*, as discussed above.

Therefore, a *prima facie* case of obviousness has not been established because any permissible combination of the cited references fails to yield all of the limitations

recited in each of independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom.

Thus, independent claims 1 and 40, and claims 7, 11-17, and 44-45, respectively depending therefrom, are patentable over *Jiang* in view of *Ikeda*, and further in view of *Chun*, and *Samukawa*. Accordingly, the Appellants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

For the reasons advanced above, Appellants respectfully urge that the rejections of claims 1 -17 and 40-45 as being unpatentable under 35 U.S.C. §103 are improper. Reversal of the rejections in this appeal is respectfully requested.

Respectfully submitted,

May 21, 2007

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CLAIMS APPENDIX

1. (Previously Presented) A method of fabricating an interconnect structure, comprising:

(a) providing a substrate having a film stack comprising sequentially formed on the substrate a first barrier layer, a conductive layer embedded in a first dielectric layer, a second barrier layer, a second dielectric layer, and a cap layer;

(b) etching a via hole in the cap layer and the second dielectric layer;

(c) filling a portion of a depth of the via hole with a masking material;

(d) etching in-situ the cap layer, a trench in the second dielectric layer, the masking material, and the second barrier layer, by providing a plasma source power of at least about 1000 Watts and a bias power of at least about 800 Watts while etching during at least a portion of step (d); and

(e) metallizing the via hole and the trench.

2. (Original) The method of claim 1 wherein the cap layer comprises SiO_xN_y , where x and y are integers.

3. (Previously Presented) The method of claim 1 wherein the first dielectric layer and the second dielectric layer comprise at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

4. (Previously Presented) The method of claim 1 wherein the first barrier layer and the second barrier layer comprise at least one of SiO_2 , SiC , and Si_3N_4 .

5. (Original) The method of claim 1 wherein the conductive layer comprises at least one of Cu, Al, Ta, W, Ti, TaN, and TiN.

6. (Original) The method of claim 1 wherein the masking material is selected from a group consisting of an organic material and photoresist.

7. (Original) The method of claim 1 wherein the step (b) further comprises:
forming a first patterned etch mask on the cap layer to define the via hole;
etching the via hole providing CF₄ and N₂ at a flow ratio CF₄:N₂ in a range from 1:1 to 1:5; and
stripping the first patterned etch mask.
8. (Original) The method of claim 1 wherein the step (c) further comprises:
applying the masking material to the substrate to fill the via hole; and
etching back the masking material until the masking material is removed from the via hole to a pre-determined depth that is smaller than a depth of the trench.
9. (Previously Presented) The method of claim 8 wherein the step (d) further comprises:
providing O₂ at a flow rate from about 100 to 1000 sccm;
maintaining a chamber pressure at about 5 to 200 mT; and
applying a cathode bias power between 100 and 400 W.
10. (Original) The method of claim 1 wherein the step (d) further comprises:
forming on the cap layer a second patterned etch mask to define the trench; and
stripping the second patterned etch mask contemporaneously with etching the masking material.
11. (Original) The method of claim 1 wherein the step (d) further comprises:
using a very high frequency (VHF) high-density plasma and a selectively controlled cathode bias power.
12. (Original) The method of claim 11 wherein the VHF is about 160 MHz.
13. (Previously Presented) The method of claim 12 wherein the cathode bias power is applied in a range from 0 to about 3000 W at a frequency in a range from about 50 kHz to 13.6 MHz during at least a portion of step (d).

14. (Original) The method of claim 11 wherein the step of etching the cap layer further comprises:

providing CF₄ and N₂ at a flow ratio CF₄:N₂ in a range from 1:1 to 1:5;
applying a source power between about 0 and 2000 W; and
applying a cathode bias power between 400 and 1200 W.

15. (Original) The method of claim 11 wherein the step of etching the trench further comprises:

providing CF₄ and N₂ at a flow ratio CF₄:N₂ in a range from 1:1.2 to 17:1;
applying a source power between about 1000 and 2000 W; and
applying a cathode bias power between 800 and 1800 W.

16. (Original) The method of claim 11 wherein the step of etching the masking material further comprises:

providing O₂ at a flow rate from about 300 to 1000 sccm;
maintaining a chamber pressure at about 5 to 200 mT;
applying a source power between about 200 and 2000 W; and
applying a cathode bias power between 100 and 400 W.

17. (Previously Presented) The method of claim 11 wherein the step of etching the second barrier layer further comprises:

providing CF₄ and N₂ at a flow ratio CF₄: N₂ in a range from 1:5 to 10:1;
applying a source power between about 200 and 600 W; and
applying a cathode bias power between 200 and 400 W.

18-39. (Cancelled)

40. (Previously Presented) A method of etching, comprising:

(a) providing a substrate having a dielectric layer to be etched on a substrate support in a process chamber, the process chamber having a plasma source electrode disposed above the substrate support and a substrate bias electrode disposed below a

support surface of the substrate support;

(b) providing an etch gas mixture; and

(c) supplying a source power of at least about 1000 Watts at a frequency of above about 100 MHz to the plasma source electrode and a bias power of at least about 800 Watts to the substrate bias electrode while etching the dielectric layer.

41. (Previously Presented) The method of claim 40, wherein the dielectric layer comprises at least one of carbon doped silicon oxide, organic doped silicon glass, and fluorine doped silicon glass.

42. (Previously Presented) The method of claim 40, further comprising:

maintaining a chamber pressure greater than about 100 mT.

43. (Previously Presented) The method of claim 40, wherein the chamber pressure is about 250 mT.

44. (Previously Presented) The method of claim 40, wherein step (c) further comprises supplying the source power at about 1,000 watts.

45. (Previously Presented) The method of claim 40, wherein step (c) further comprises providing the bias power at about 1,800 watts.

EVIDENCE APPENDIX

[NONE]

RELATED PROCEEDINGS APPENDIX

[NONE]